

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device, comprising:

a semiconductor substrate;

a semiconductor element formed on said semiconductor substrate by overlaying a plurality of patterned layers; and

a position check mark used for overlay of said plurality of layers,

wherein said semiconductor element includes:

an interlayer insulating film formed on said semiconductor substrate;

a contact hole penetrating said interlayer insulating film to reach said semiconductor substrate;

a plug that is conductive and fills said contact hole;

a barrier metal layer provided to cover said contact hole and to be electrically connected to said plug; and

a conductive film formed on said barrier metal layer, and wherein said position check mark includes:

a plurality of mark holes formed to penetrate said interlayer insulating film;

a plurality of recess plug plugs that is are conductive and provided so that its their respective one end portion portions on a side opposite to said semiconductor substrate is are recessed in said plurality of mark holes;

and wherein said barrier metal layer is provided to cover said plurality of mark holes and to be electrically connected to said recess plug; and
said conductive film is formed on said barrier metal layer.

Claim 2 (Currently Amended): The semiconductor device according to claim 1, wherein an opening size of each of said plurality of mark holes ranges from ~~almost~~ substantially as large as an opening size of said contact hole to ~~almost~~ substantially twice as large as the opening size of said contact hole.

Claim 3 (Original): The semiconductor device according to claim 1, wherein said plurality of mark holes are formed through a same process as said contact hole.

Claim 4 (Currently Amended): A semiconductor device, comprising:
a semiconductor substrate;
a semiconductor element formed on said semiconductor substrate by overlaying a plurality of patterned layers; and
a position check mark used for overlay of said plurality of layers,
wherein said semiconductor element includes:
an interlayer insulating film formed on said semiconductor substrate;
a contact hole penetrating said interlayer insulating film to reach said semiconductor substrate;
a plug that is conductive and fills said contact hole;
a barrier metal layer provided to cover said contact hole and to be electrically connected to said plug; and
a conductive film formed on said barrier metal layer,
and wherein
said position check mark has a recess region in which a determined region of said interlayer insulating film is recessed;

a plurality of mark holes are formed to penetrate said interlayer insulating film in said recess region;

a plurality of protrusion plug plugs that is are conductive is are provided so that its their respective one end portion portions on a side opposite to said semiconductor substrate protrudes protrude from said plurality of mark holes;

said barrier metal layer is provided to cover said plurality of mark holes and to be electrically connected to said protrusion plug; and

said conductive film is formed on said barrier metal layer.

Claim 5 (Currently Amended): The semiconductor device according to claim 4, wherein

an opening size of each of said plurality of mark holes ranges from almost substantially as large as an opening size of said contact hole to almost substantially twice as large as the opening size of said contact hole.

Claim 6 (Original): The semiconductor device according to claim 4, wherein said plurality of mark holes are formed through a same process as said contact hole.

Claims 7-19 (Canceled).